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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
JOHNSON, RYAN	

ART UNIT	PAPER NUMBER
2817	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/589,133	KOUKAB ET AL.	
	Examiner	Art Unit	
	Ryan J. Johnson	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-21 and 23-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *28-36* is/are allowed.

6)☒ Claim(s) *19-21,23,26,37-39,43 and 45* is/are rejected.

7)☒ Claim(s) *24,25,27,40-42 and 44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the amendment received April 4th, 2008. Claims 19-21 and 23-45 are pending. Claims 1-18 and 22 are cancelled. Claims 19-21 and 23-36 have been amended. New claims 37-45 have been added. As a result of the amendments, the rejection of claims 19-36 under U.S.C. 112 2nd paragraph has been withdrawn. The abstract has been amended, thus the objection to the abstract is withdrawn.

Response to Arguments

2. Applicant's arguments filed April 4th, 2008 have been fully considered but they are not persuasive. Applicant argues, with respect to claim 19, Allot and Iadanza et al. do not show, teach, or suggest switching a VCO operating mode to a linear-high-gain mode to enable a first frequency tuning operation that includes targeting a linear frequency versus voltage curve to vary frequency output of the VCO within a frequency locking range. The Examiner disagrees. As admitted in the prior action, Allot (U.S. Patent No. 6,747,521, as cited in the previous action) does disclose that the frequency-voltage curve of the oscillator is linear. However, as discussed further below and in the prior action, targeting a linear portion of a VCO curve is well known in the art. Iadanza et al. (U.S. Publication No. 2004/0263259, as cited in the previous action and hereinafter "Iadanza") discloses that utilizing (i.e. targeting) a linear portion of the frequency-voltage curve results in an improved level of control (see [0004],[0007]).

3. Applicant argues that "Iadanza does not use, target or follow a f/v curve during operation of a VCO. As best understood by Applicants, Iadanza discloses a VCO that

has a corresponding non-linear f/v performance curve." This argument is not persuasive. Iadanza discloses that most oscillators in a PLL seek to utilize (i.e. target) a linear f/v curve in order to provide “the highest level of control over the oscillating loop structure". The Examiner notes that claim 19 does not explicitly require the entire VCO curve to be linear. Claim 19 recites, "switching a voltage-controlled oscillator operating mode to a linear-high-gain mode to enable a first frequency tuning operation that includes targeting a linear frequency versus voltage curve to vary the frequency of the output signal within a frequency locking range". Since Iadanza discloses that targeting a linear frequency curve of an oscillator is often done in order to provide a higher level of loop control, it would have been obvious to target a linear portion of the oscillator f/v curve of Allot in order to have provided such control. The Examiner also notes that the Applicant admits that Iadanza discloses utilizing (i.e. targeting) a linear f/v curve. Page 3, Lines 8-10 of the present arguments reads, "Iadanza appears to disclose the adjusting of a control parameter value of the VCO such that the VCO is operated in a linear range of the non-linear curve.

4. The Applicant further argues, “The operation of Iadanza significantly narrows the operating range of frequencies. By operating in a linear portion of a non-linear curve, the range of frequencies that a PLL can lock onto is narrowed." This argument is not commensurate with the scope of the claim. The claim language does not require that the VCO curve be entirely linear; the claim only requires that a linear portion of the curve is "targeted". Such targeting of a linear f/v curve is well-known in the art.

5. Finally, the Examiner notes that assuming, *arguendo*, that Iadanza did not teach targeting a linear f/v curve, such targeting is well known in the art, and often a design requirement of a VCO in a PLL in order to provide superior loop control and, as a result, improved phase noise characteristics (see Justice et al. --- U.S. Patent No. 6,596,075, as cited in the previous action --- Figs.3,4 and 6 for additional examples of targeting linear f/v curves).

Claim Rejections - 35 USC § 112

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claim 43 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the relationship between the recited "an offset generator" with the remainder of the PLL system.

Claim Rejections - 35 USC § 103

8. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

9. Claims 19, 20, 26, 37-39, 43, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allott in view of Iadanza.

10. Regarding claims 19 and 22, Allot discloses a method for analogue self calibrating of a phase locked loop circuit (Figs.6,9) including a phase frequency detector (133), a charge pump (137,138), a loop filter (144), a voltage controlled oscillator (145),

including elements (220,224,234; Fig.7) tuned by a tuning voltage (V1), the method comprising:

comparing a frequency of an output signal of the VCO of the phase-locked loop circuit with a reference signal frequency entering in the PFD (the PFD compares the output of the VCO --151, through divider 149 -- with the reference frequency 131);

switching a voltage-controlled oscillator operating mode, in a first frequency tuning operation enabling to wide locking range, to a high gain mode (step 303; col.11,46-49; col.8,34-47); and

automatically switching, after locking to an appropriate frequency with the first tuning operation (lock is achieved in step 307; col.57-59), said voltage controlled oscillator operating mode to a zero-gain mode, while keeping the frequency of the voltage controlled oscillator unchanged (in sleep mode, the output voltage V2 is latched, PLL circuitry is shut down, and the oscillator maintains its frequency; col.11,61-col.12,5; col.9,11-29).

11. Allott does not explicitly disclose that the frequency-voltage curve is linear. The Examiner notes that using the linear portion of the frequency-voltage curve of a VCO is well known in the art. Iadanza et al. discloses that utilizing the linear portion of the frequency-voltage curve results in an improved level of control ([0004],[0007]). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the linear portion of the frequency-voltage curve of the VCO of Allott, as disclosed by Iadanza et al., in order to have provided the benefits of improved oscillator control.

12. Regarding claim 20, Allott discloses that after said zero-gain mode, said voltage controlled oscillator operating mode is switched to a low gain mode enabling a fine tuning of the frequency by the phase locked loop for compensating small residual frequency errors (after sleep mode is disengaged --step 315--, the system returns to normal operation and low gain, integrating mode is enabled --step 307 following steps 301,303 and 305).

13. Regarding claim 26, Allot discloses that the lock time is improved by increasing the current of the charge pump (During coarse tuning, the first charge pump 137 is used, which has a current 10 times the second charge pump; col.8,65-col.9,10).

14. Regarding claims 37-39, Iadanza discloses targeting a linear portion of the VCO curve in order to provide improve loop control, as discussed above. Therefore, since a linear portion of the oscillator is targeted, the VCO maintains a constant gain (i.e. a constant f/v curve), and the tuning voltage is configured in order to maintain said gain (for further explanation, see above).

15. Regarding claim 43, during zero gain mode, Allot discloses isolating the VCO from the rest of the loop, including an offset generator (the charge pump 137,138 offsets the loop filter voltage). Although Allot does not explicitly disclose the use of a varactor in the VCO, the Examiner takes Official Notice that such varactors are well known tuning mechanisms within a VCO of a PLL and merely providing a suitable VCO with a tuning varactor to the circuit of Allot would require only routine skill in the art.

16. Regarding claim 45, Allot discloses providing a constant voltage to the VCO while in zero-gain mode. Although Allot does not explicitly disclose a capacitance within

the VCO, such a varactor is well known in the art, as discussed above. The Examiner notes that by using a conventional VCO with a varactor within the circuit of Allot, a constant capacitance would be achieved when a constant voltage would be applied to the VCO.

17. Claims 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allott in view of Iadanza as applied to claim 19 above, and further in view of Justice et al. (U.S. Patent No. 6,496,075, as cited in the previous action and hereinafter "Justice"). Allot and Iadanza et al. disclose the limitations of claim 19. Allot also discloses isolating the elements from their controlling voltages when the phase locked loop is locked (during sleep while the loop is locked, the memory cell 207 outputs a constant voltage, thus isolating itself from V1) and freezing the elements in a state previously obtained to activate zero-gain mode (memory cell 207 outputs a constant voltage, freezing V2 and the analog memory cell output). Neither Allott or Iadanza et al. discloses breaking the linear frequency-voltage curve into several sections, selecting for each section a corresponding element, or submitting each element to a specific voltage, as required by claim 21, or comparing each element to a reference voltage and depending on the result of the comparison, applying a voltage to each element, as required by claim 23. Justice et al. discloses (Fig.7) using comparators (52) comparing a reference voltage (50) to the tuning voltage output (Vtune). Voltages are output from logic (54) to switches (32) in order to enable capacitors (34). Justice discloses that such a structure between the loop filter and VCO provides an extension of the linear tuning

range with low phase noise (col.6,24-61; Fig.6). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the control circuit, including comparators, reference voltages, logic, and switched capacitors, as disclosed by Justice et al., between the tuning voltage and VCO in the circuit of Allott in order to have provided the benefits of a wide tuning range with low phase noise.

Allowable Subject Matter

18. Claims 28-36 are allowed. See the previous Office Action.

19. Claims 24, 25 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. See the previous Office Action.

20. Claims 40-42 and 44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: Regarding claims 40-42, the recited comparison and offsetting limitations could not be found in the prior art within the overall context of the claims. Regarding claim 44, “comparing an offset control voltage to a reference voltage; and setting the tuning voltage to one of a plurality of voltage potentials base on said comparing" could not be found in the prior art within the overall context of the claims.

Conclusion

21. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan J. Johnson whose telephone number is (571)270-1264. The examiner can normally be reached on Monday - Thursday, 9:00 am - 5:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RJJ/

/Robert Pascal/
Supervisory Patent Examiner, Art Unit 2817